active and passive circuit parameters," *NBS Tech. Note 673*, Sept. 1975.
[6] G. F. Engen, "The six-port reflectometer: an alternative network analyser," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-25, pp. 1075–1083, Dec. 1977.
[7] D. Woods, "Analysis and calibration theory of a general 6-port reflectometer employing four amplitude detectors," *Proc. Inst. Elec. Eng.*, vol. 126, pp. 221–228, Feb. 1979.
[8] B. O. Weinschel, "Six-port sceptic," *Microwaves*, (*Corresp.*), vol. 19, pp. 11–12, Oct. 1980.
[9] G. F. Engen, "Calibrating the six-port reflectometer by means of sliding terminations," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 951–957, Dec. 1978.
[10] P. I. Somlo, "The locating reflectometer," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-20, pp. 105–112, Feb. 1972.
[11] G. F. Engen and R. W. Beatty, "Microwave reflectometer techniques," *IRE Trans. Microwave Theory Tech.*, vol. MTT-7, pp. 351–355, July 1959.
[12] P. I. Somlo, "Automated measurement of noisy voltages with a preset confidence level," *Electron. Lett.*, vol. 13, pp. 234–235, April 1977.

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P. I. Somlo (SM'71) was born in Budapest, Hungary, in 1933. He graduated from the University of Technology of Budapest in 1956. After graduation he joined the Fine Mechanics Company, Budapest, where he was engaged in the development and design of high frequency laboratory equipment. In 1957 he joined the Standard Telephones and Cables Company, London, England, where his work was concerned with microwave repeater stations. In 1957 he joined the Standard Telephones and Cables Company, Liverpool, N.S.W., Australia, where he was engaged in developing pulse-technique circuitry. In the same year he joined the National Measurement Laboratory, Division of Applied Physics of Commonwealth Industrial and Research Organization (CSIRO) of Australia, where he is a Principal Research Scientist, Head of the RF/Microwave Group. His work includes the design and operation of radio frequency and microwave standards of measurement and the development of associated measuring techniques. He is the author of a number of articles and is the joint inventor of three patents.

Since 1970 Mr. Somlo has been a member of the *IEEE Trans. MTT* Editorial Review Borad, and is Vice Chairman of the IEEE Australian Section.

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John D. Hunter (S'68–M'79) received the B.E. (Hons.) and Ph.D. degrees in electrical engineering from the University of Canterbury, New Zealand, in 1967 and 1970, respectively.

After teaching at the University of Canterbury from 1970–71, he worked on electromagnetic scattering problems as a Post-Doctoral Fellow with the University of Manitoba, Winnipeg, Canada, from 1971–73. He is currently a Senior Research Scientist with the CSIRO Division of Applied Physics, Sydney, Australia, and is working on the improvement of measurement techniques at radio and microwave frequencies.

Short Papers

A Broad-Band Amplifier Output Network Design

ALFY N. RIDDLE AND R. J. TREW, MEMBER, IEEE

Abstract—**An analytic design method for a lossy gain-compensating network is presented and the advantages of lossy networks are discussed. Examples of two-stage amplifiers using FET's and bipolar transistors are presented to show the feasibility of this particular network in low power amplifier designs. These amplifiers obtain gains of 15.4±0.5 dB with a 2.5-dB maximum noise figure in the 4.0–6.0-GHz frequency range and 16.5±1.2 dB with a maximum input VSWR of 1.78:1 over the 1.0–2.0-GHz frequency range, respectively.**

I. Introduction

Lossy gain-compensating output networks can provide lower input reflection coefficients, a lower amplifier noise figure, and a more predictable amplifier design [1]. The resistive nature of this type of network may also improve amplifier stability and distortion by reducing standing waves within the amplifier. Although lossy broad-band gain-compensating networks are often used [1]–[4], explicit, analytic design techniques for these networks have not been reported.

This paper presents an output circuit design based upon a π matching network combined with a bandpass/bandstop diplexer. As a result, this network contains both the drain supply inductance and the dc blocking capacitor, which are needed in any output network, as integral elements. Explicit formulas for the element values of this network are derived and presented shortly. This method is different from previous methods [1] because this technique allows the device load to approach 50 Ω as frequency is decreased. However, this network is similar to that used in [2] and [3] in that the supply voltage is inserted through a quarter-wavelength shunt stub and a series resistor. This method results in greater stability and tunability for the amplifier.

A bandpass/bandstop diplexer is more useful than a simple low-pass/high-pass diplexer because it provides an exact match at one frequency, and an arbitrary amount of attenuation (limited only by network element Q's) at any frequency. Diplexing networks may be used in either input or output networks depending

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The authors are with the Department of Electrical Engineering, North Carolina State University, Raleigh, NC 27650.

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on noise figure, power output, stability, and other amplifier constraints. This paper considers the characteristics of a resonant diplexer in the output network.

II. Network Design

The output network is designed in two parts. First, a π network matches the transistor output impedance to 50 Ω at the highest frequency of interest f_H. The insertion loss of this network IL_p, at the lowest frequency of interest f_L, is calculated and subtracted from the total loss desired for gain compensation IL_T to give the loss required of the diplexer IL_d. This may be expressed as

$$IL_T(f_L)=IL_d(f_L)+IL_p(f_L)=MAG(f_L)-MAG(f_H) \quad (1)$$

where $IL_T(f_H)=0=IL_d(f_H)=IL_p(f_H)$, and $MAG(f)$ is the maximum available gain of the device and input network at the specified frequency. In this paper, insertion loss is in decibels, and is with respect to the maximum power available from a 50-Ω source. This simple two-point method of compensation works well for the gradual gain versus frequency slopes of single-stage amplifiers. The diplexer center frequency is f_H, and the diplexer bandwidth is determined by the required loss IL_d, at f_L.

A standard parallel RC network equivalent circuit is derived for the transistor output impedance. This circuit may be derived in a conventional manner from $S_{22}(f_H)$ in the unilateral case, from the conjugate of the output match reflection coefficient for minimum noise at f_H, or from the conjugate of the complete match reflection coefficient at f_H. In the π matching network shown in Fig. 1, R_0 and C_1 are derived from the transistor output admittance. It is worth noting that L_2 consists, at least in part, of the bonding wire to the transistor chip from the microstrip circuit. The equations for this matching network are derived by separating the network at node A in Fig. 1 and writing expressions for the impedances looking towards R_0 and R_L. Real and imaginary (one direction being conjugated) parts are equated to obtain a match. Thus, we have

$$Q_0=\omega_H R_0 C_1 \quad (2)$$

$$Q_L=\omega_H R_L C_3=\left[\frac{R_L}{R_0}\left(Q_0^2+1\right)-1\right]^{1/2} \quad (3)$$

$$C_3=\frac{Q_L}{\omega_H R_L} \quad (3a)$$

$$L_2=\left[\frac{R_0^2 C_1}{1+Q_0^2}+\frac{R_L^2 C_3}{1+Q_L^2}\right] \quad (4)$$

where $\omega_H=2\pi f_H$.

The insertion loss for this network may be derived by describing the network as an $ABCD$ matrix seen from R_L. The matrix elements may be converted to S-parameters via the relation [5]

$$S_{21}(j\omega)=\frac{2\sqrt{R_0 R_L}}{A(j\omega)R_0+D(j\omega)R_L+B(j\omega)+C(j\omega)R_0R_L} \quad (5)$$

and expressed as an insertion loss in decibels by

$$IL_p(j\omega)=10\log|S_{21}(j\omega)|^2$$

$$=10\log\left(\frac{4R_0R_L}{\left[R_0+R_L-\left(\frac{\omega}{\omega_H}\right)^2X_2(Q_0+Q_L)\right]^2+\left[\frac{\omega}{\omega_H}\left\{X_2+R_LQ_0+R_0Q_L-\left(\frac{\omega}{\omega_H}\right)^2X_2Q_0Q_L\right\}\right]^2}\right) \quad (6)$$

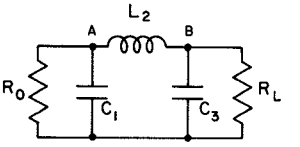


Fig. 1 π matching network. R_0 and C_1 are the transistor output equivalent circuit.

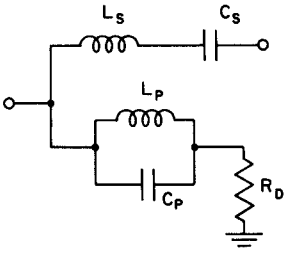


Fig. 2. Resonant diplexer network for lossy gain compensation.

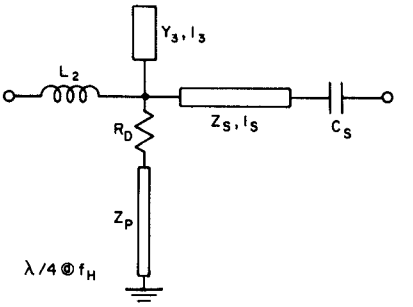


Fig 3 Distributed form of output network for lossy gain compensation

where $X_2=\omega_H L_2$. Since the diplexer presents a constant 50 Ω to this network, this insertion loss is affected mainly by changes in the elements of the transistor output equivalent circuit. The FET design shown later suffered very little from an 85-percent change in its output conductance across the operating frequency range. In these situations an average output conductance weighted toward the top of the frequency range may be useful. The mismatch of the π network at f_L has not been found to disturb the diplexer's characteristics. The desired diplexer loss IL_d, at f_L determines the diplexer bandwidth by the relation

$$BW=\frac{f_H^2-f_L^2}{f_Hf_L\left(10^{IL_d/10}-1\right)^{1/2}} \quad (7)$$

which comes from the expression

$$IL_d=10\log\frac{1}{1+\left[\frac{1}{BW}\left(\frac{f_H^2-f_L^2}{f_Hf_L}\right)\right]^2} \quad (7a)$$

where IL_d is a positive number and the bandwidth BW is normalized. This equation is a rearranged form of the insertion loss for a simple resonant network. The equations presented below for the diplexer in Fig. 2 may be found in any network synthesis text [6]

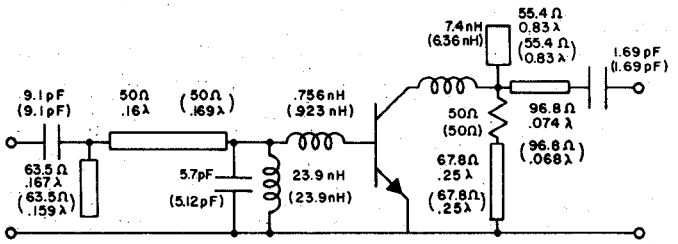
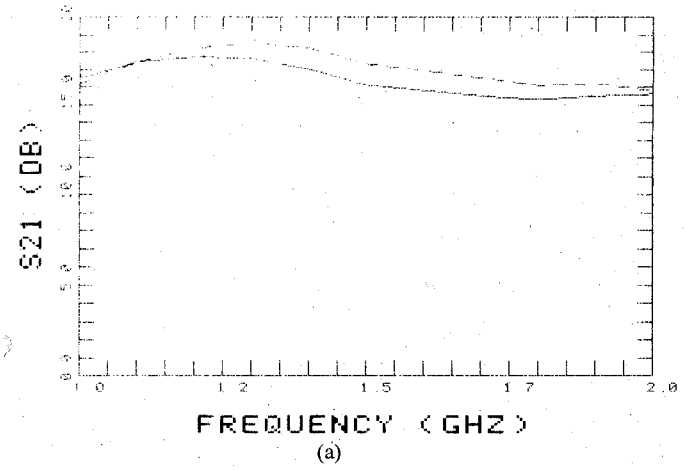
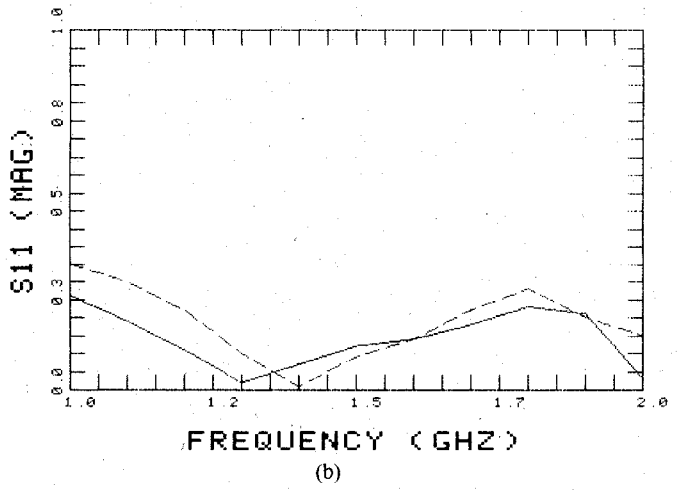


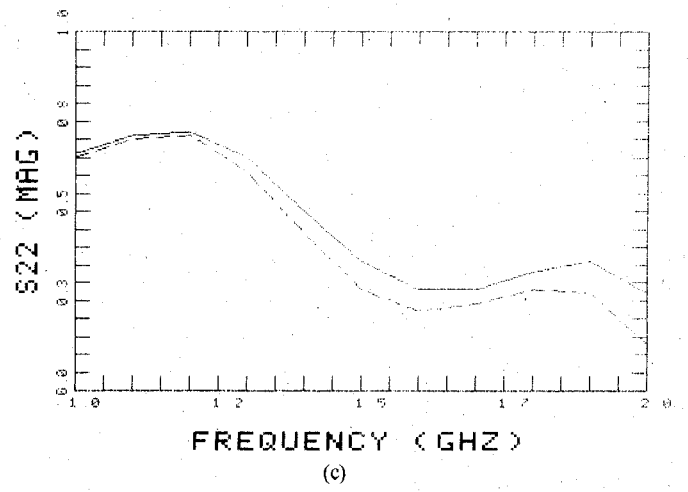
Fig. 4. MRF901 amplifier design for 1.0- to 2.0-GHz frequency range. All line lengths are a fraction of a wavelength to 2.0 GHz. Optimized values are in parenthesis.



(a)



(b)



(c)

Fig. 5. MRF901 1.0–2.0-GHz amplifier characteristics. (a) S_{21}(db). (b) $|S_{11}|$. (c) $|S_{22}|$.

$$C_S = \frac{BW}{50\omega_H} \tag{8a}$$

$$L_S = \frac{1}{\omega_H^2 C_s} = (50)^2 C_p \tag{8b}$$

$$L_p = \frac{BW(50)}{\omega_H} = (50)^2 C_S \tag{8c}$$

$$C_p = \frac{1}{\omega_H^2 L_p}. \tag{8d}$$

In the final network, the diplexer replaces R_L of Fig. 1 and the output of the amplifier is taken from the diplexer's series LC circuit. Fig. 3 shows the entire output network in distributed form; with $Z_p = 4\omega_H L_p/\pi$, $Z_S = \omega_H L_S/\tan(2\pi l_S/\lambda)$, and $Y_3 = \omega_H C_3/\tan(2\pi l_3/\lambda)$, where l is the transmission-line length. These lumped to distributed network equivalences are derived by equating reactance slopes of the elements at the desired center frequency [7].

III. Examples

Amplifier designs using a Motorola MRF901 and a Hewlett-Packard HFET-1101 are shown in Figs. 4–7. These designs were analyzed and optimized with COMPACT. Figs. 4 and 6 show the

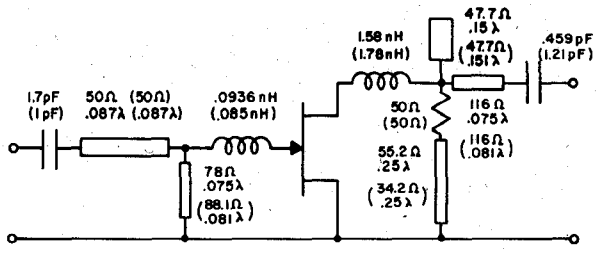
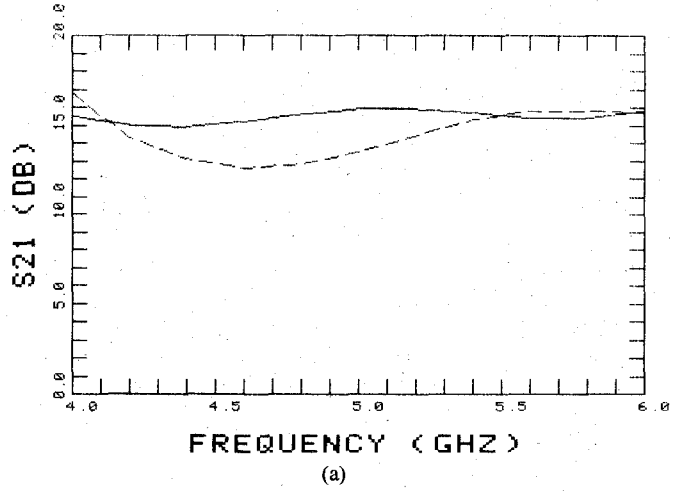
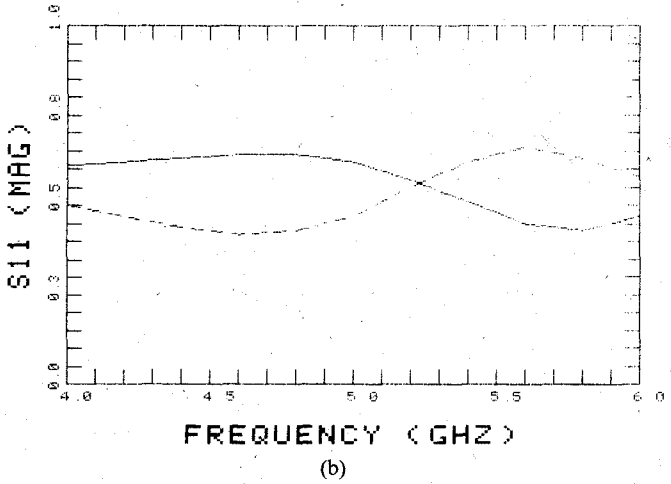


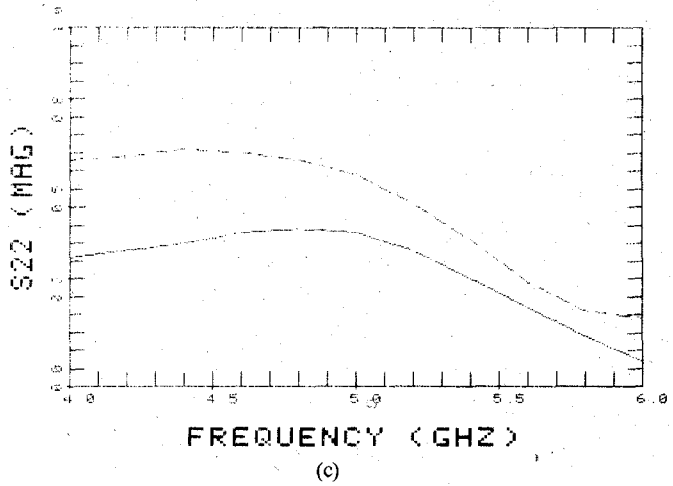
Fig. 6. HFET-1101 amplifier designed for minimum noise figure in the 4.0- to 6.0-GHz frequency range. All lines are given in a fraction of a wavelength at 6.0 GHz. Optimized values are in parenthesis.



(a)



(b)



(c)

Fig. 7. HFET-1101 4.0–6.0-GHz low-noise amplifier characteristics. (a) S_{21}(db). (b) $|S_{11}|$. (c) $|S_{22}|$.

actual designs with optimized element values in parenthesis. Figs. 5 and 7 show the characteristics of a two-stage cascade of each amplifier before and after optimization, with the solid lines representing optimization.

The MRF901 amplifier was designed for minimum input reflection coefficient and maximum flat gain over the 1.0 to 2.0-GHz frequency range. The equivalent circuit for this device was based on a complete conjugate match at 1.0 and 2.0 GHz. Because this transistor's input circuit appeared as a dominantly inductive series-resonant circuit, an iterative Smith Chart procedure was used to design the input network. The output network was designed according to the equations of the previous section. Since the *MAG* of the MRF901 was 8.0 dB at 2.0 GHz and 13.8 dB at 1.0 GHz, 5.8 dB of insertion loss was required of the output network at 1.0 GHz. This insertion loss was composed of 1.05 dB of π network loss and 4.75 dB of diplexer loss. The diplexer loss of 4.75 dB determined a bandwidth of 1.065. Figs. 4 and 5 indicate that this design was easily cascaded and required no optimization. Lossless gain-compensating output networks were tried with this combination of device and input network with less predictable results. Figs. 5(a), (b), and (c) show maximums of ± 1.4 dB of gain variation around 16.8-dB gain, 1.78:1 input VSWR, and 6.2:1 output VSWR.

The HFET-1101 amplifier was designed for minimum noise

figure in the 4.0 to 6.0-GHz frequency range with a maximum flat gain. The analytic approach used in [2] was the basis of the input network design. This input network was designed to match the conjugate of the optimum source impedance for low noise at 5.0 GHz. Interpolation was used to derive this impedance from the published data at 4.0 and 6.0 GHz. The network element values were derived from an $n=3$, 0.01-dB ripple, Chebyshev low-pass prototype [8]. The first impedance inverter (K_{34}) was omitted from the final design because its 50.75 Ω impedance contributed little to the overall match.

The transistor output equivalent circuit was derived from the conjugate of the reflection coefficient for a matched output with minimum noise. The unilateral gain approximation as described in [9] was used to find the maximum amplifier gain at 4.0 and 6.0 GHz. The source reflection coefficient derived from the conjugate of the transistor input equivalent circuit at 4.0 and 6.0 GHz was used in this unilateral gain approximation. This required 3.55 dB of loss at 4.0 GHz. A maximum gain of 8.45 dB at 6.0 GHz was expected for the amplifier. The diplexer network needed to provide 2.85 dB of the 3.55-dB loss, and so a normalized bandwidth of 0.864 was used. Although the cascade of two identical single-stage amplifiers provided acceptable results without adjustment of any of the circuit elements, optimization improved the gain flatness and output reflection coefficient. The noise figures of 2.1 dB and 4.0 GHz and 2.35 dB at 6.0 GHz were changed to 1.9 dB at 4.0 GHz and 2.48 dB at 6.0 GHz during optimization. The relatively high VSWR of this amplifier's input, as shown in Fig. 7(b), is due to providing an optimum source impedance for noise minimization.

The formulas presented in this paper are useful whenever the equivalent circuit of the device is a parallel *RC* network. Therefore, bipolar transistor amplifiers operating well below the device's f_T may contain the circuit just presented as an input matching network.

IV. Conclusion

A simple output network was shown to simultaneously provide gain-compensation and a predictable amplifier design. The feasibility of this design method was demonstrated by cascading two identical single-stage amplifiers and calculating the total amplifier *S*-parameters before and after optimization. Although the input and output networks were designed by treating the amplifier as if these networks did not interact, the actual results agreed well with simple theory. Explicit formulas for the design of lumped and distributed output networks were presented.

Acknowledgment

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References

[1] Noel Marshall, "Optimizing multi-stage amplifiers for low-noise," *Microwaves*, pp. 62–64, Apr. 1974, pp. 60–64, May 1974.
[2] C. A. Liechti and R. L. Tillman, "Design and performance of microwave amplifiers with GaAs Schottky-Gate field-effect transistors," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 510–517, May 1974.
[3] D. P. Hornbuckle and L. J. Kuhlman, Jr., "Broad-Band medium-power amplification in the 2–12.4-GHz range with GaAs MESFET's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 338–342, June 1976.
[4] Charles A. Liechti, "Microwave field-effect transistors-1976," *IEEE Trans Microwave Theory Tech.*, vol. MTT-24, pp. 279–298, June 1976.
[5] M. A. R. Gunston, *Practical Matrix Algebra*. New York: Elsevier, 1970, p 127.
[6] F F. Kuo, *Network Analysis and Synthesis* New York. Wiley, 1966, p. 406.
[7] George L. Ragan, *Microwave Transmission Circuits* New York: Dover, 1965, p 617.
[8] Anatol I Zverev, *Handbook of Filter Synthesis*. New York: Wiley, 1967, p 315
[9] *S-Parameter Design*, Hewlett-Packard Company HP Application Note 154, Apr. 1972, p. 25.

Application of the Galerkin Method for Determination of Quasi TE_{i0k} Mode Frequencies of a Rectangular Cavity Containing a Dielectric Sample

ANDRZEJ KEDZIOR AND JERZY KRUPKA

***Abstract*—A new method determination of quasi TE_{i0k} mode frequencies of a rectangular cavity containing a dielectric sample is presented. A centrally loaded dielectric sample fills completely only one dimension of a cross section of the cavity. The calculations are based on the Galerkin method using a new suitable set of basis functions. The theoretical results are illustrated by experiments. The obtained results of calculations and experiments demonstrate the advantages of the new basis as compared with the classical one. The presented method may be applied for the analysis of two-dimensional boundary problems for various resonant cavities with inhomogeneous filling.**

I. Introduction

It is often necessary to determine the permittivity of rectangular samples of precisely defined dimensions at microwave frequencies. The parameters of such samples are determined most frequently by resonance method. The form of the sample determines the rectangular form of the cavity [2],[4],[5]. An accurate determination of the permittivity of precisely defined dimension samples is often difficult, especially at the low microwave frequencies. At these frequencies cavity dimensions are usually larger than respective sample dimensions. This leads to the necessity of using approximate methods for determining the resonant frequency of the cavity in relation to the permittivity. Since it is easier to determine the resonant frequency of the cavity at a fixed permittivity, the paper presents the solution of such problems.

II. Theory

In this section is presented a method of determining the angular frequencies of quasi TE_{i0k} modes ($i, k =$ odd numbers) of rectangular cavity with infinity conducting walls, filled with a dielectric in the way shown in Fig 1(a). This problem is reduced to determination of the eigenvalues of the boundary problem

$$L\phi = j\omega M\phi$$
$$\boldsymbol{n}\times\boldsymbol{E}=0, \qquad \text{on } S \tag{1}$$

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The authors are with the Instytut Technologii Elektronowej, Politechniki Warszawskiej ul. Koszykowa 75, 00-662 Warszawa, Poland

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